



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/841,270	04/24/2001	Steven A. Guccione	X-806 US	6015
24309	7590	04/07/2004	EXAMINER	
XILINX, INC ATTN: LEGAL DEPARTMENT 2100 LOGIC DR SAN JOSE, CA 95124			CHANDRASEKHAR, PRANAV	
			ART UNIT	PAPER NUMBER
			2115	3
DATE MAILED: 04/07/2004				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/841,270	GUCCIONE ET AL. <i>Jm</i>	
	Examiner	Art Unit	
	Pranav Chandrasekhar	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 24 April 2001.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-17 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1,6-13 and 15-17 is/are rejected.
- 7) Claim(s) 2-5 and 14 is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: _____

DETAILED ACTION

Claim Objections

1. Claims 2 and 11 are objected to because of the following informalities:

As per line 10 of claim 2, 'subsequent' has been misspelled as 'subsequently'.

As per claim 11, the claim is an exact repetition of claim 10.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1,6-12,13 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mason et al [US Pat No. 5,946,219] in view of Lomet et al [US Pat No. 5,524,205].

3. As per claim 1, Mason teaches

executing on the host arrangement a run-time reconfiguration program [col. 6 lines 24-25. The system for reconfiguring the device is viewed as a host on which a reconfiguring program is being executed] that, via the programming interface, specifies a circuit design [col. 6 lines 26-30], generates configuration data that implements the

Art Unit: 2115

circuit design on the PLD [col. 6 lines 29-32], and configures the PLD with configuration data [col. 6 lines 1-10];

saving a copy of the configuration data on the host arrangement via the programming interface [col. 6 lines 29-32];

activating the PLD [The PLD is viewed as being activated prior to being configured];

updating selected portions of the configuration data via the programming interface [col. 6 lines 34-41];

automatically and partially reconfiguring the PLD responsive to the run-time reconfiguration program on the basis of the modified portions [col. 15 lines 12-18].

Mason does not explicitly teach designating portions of the configuration data that have been changed in the updating step as dirty portions via the programming interface. Furthermore, Mason does not teach automatically selecting dirty portions of configuration data for partial reconfiguration of the PLD in response to the run-time reconfiguration program.

Lomet teaches designating dirty portions of data in a dirty block table and only scanning these portions of a storage medium as dictated by the dirty block table [col. 13 lines 17-24; col. 13 lines 62-64; col. 5 lines 28-32].

It would have been obvious to combine the teachings of Mason and Lomet to partially reconfigure the PLD only on the basis of modified portions of the configuration data on the host as dictated by designated dirty portions in order to minimize the time

Art Unit: 2115

taken to reconfigure the programmable logic device by avoiding a complete reconfiguration of the programmable logic device.

4. As per claim 12, Mason teaches

means for executing a run-time reconfiguration program that includes executable code that specifies a circuit design [col. 6 lines 24-30]. The program is viewed as including executable code that specifies the circuit design.], generates configuration data that implements the circuit design on the PLD [col. 6 lines 29-32], and configures the PLD with the configuration data [col. 6 lines 1-10];

means for saving a copy of the configuration data on the host arrangement [col. 6 lines 29-32];

means for activating the PLD [The PLD is viewed as having means to be activated prior to being configured];and

means for updating selected portions of the configuration data via execution of the run-time reconfiguration program [col. 6 lines 34-41].

Mason does not explicitly teach means for updating selected portions of the configuration data as dirty portions; and automatically selecting the dirty portions of the configuration data for partially reconfiguring the PLD responsive to the run-time configuration program.

Lomet teaches

means for updating selected portions of the data as dirty portions and automatically selecting the dirty portions of the data for changing the portions to be modified [col. 13 lines 17-24; col. 13 lines 62-64; col. 5 lines 28-32].

5. As per claim 13, Mason teaches

a programmable logic device [col. 6 lines 24-25] ;
a host data processing arrangement coupled to the programmable logic device and configured with a run-time reconfiguration program and a run-time reconfiguration programming interface [col. 6 lines 23-29], wherein the run-time reconfiguration program includes executable code that invokes the programming interface to specify a circuit design [col. 6 lines 26-29], generates configuration data that implements the circuit design on the PLD [col. 6 lines 29-34], and configures the PLD with the configuration data [col. 6 lines 1-10]; and

wherein the programming interface is further configured, responsive to calls from the run-time reconfiguration program, to save a copy of the configuration data, activate the PLD [col. 6 lines 26-34] and update selected portions of the configuration data [col. 6 lines 36-38] and automatically selecting the modified portions of the configuration data for partially reconfiguring the PLD [col. 15 lines 12-18].

Mason does not explicitly teach designating updated portions of the configuration data as dirty portions, and automatically selecting dirty portions for partially reconfiguring the PLD.

Lomet teaches designating portions of data as dirty portions, and automatically selecting the dirty portions to make appropriate modifications to the persistent storage medium during data recovery [col. 13 lines 17-24; col. 13 lines 62-64; col. 5 lines 28-32].

6. As per claims 6 and 15, Mason further teaches

reading from a designated source configuration data corresponding to selected programmable portions of the PLD, wherein the configuration data from the designated source is read-in data [col. 6 lines 35-39];

updating the copy of the configuration data on the host arrangement with the read-in data [col. 6 lines 38-43].

Mason does not explicitly teach designating portions of the copy of the configuration data changed with the read-in data as dirty portions.

Lomet teaches designating portions of read-in data that have been changed as dirty portions [col. 17 lines 17-24; col. 5 lines 28-32].

7. As per claims 7, 9 and 16, Mason further teaches selecting the modified portions, assembling a partial configuration bitstream containing at least one of the modified portions and transmitting the bitstream to the PLD [col. 6 lines 39-44].

Mason and Lomet do not explicitly teach assembling one or more packets wherein each packet contains a configuration command.

It would have been obvious to modify the teachings of Mason and Lomet to assemble one or more packets and incorporate a configuration command within each of the packets to reconfigure the PLD.

8. As per claims 8,10,11 and 17, Lomet further teaches establishing a dirty frame map in memory of the host arrangement, wherein a value of each entry in the map indicated whether a corresponding frame of the PLD is dirty [col. 13 lines 17-24].

Art Unit: 2115

Mason and Lomet do not explicitly teach the PLD including a plurality of configurable logic blocks and being partially configurable in units of one or more frames, each frame including a plurality of CLBs.

It would have been obvious to modify the teachings of Mason and Lomet to enable the PLD to include a plurality of configurable logic blocks and to be partially configurable in units of one or more frames.

Allowable Subject Matter

9. Claims 2-5 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pranav Chandrasekhar whose telephone number is 703-305-8647. The examiner can normally be reached on 8:30 a.m.-5:00 p.m..

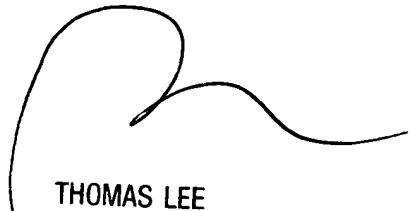
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 703-305-9717. The fax phone numbers for the organization where this application or proceeding is assigned are 703-

Art Unit: 2115

746-7239 for regular communications and 703-746-7238 for After Final
communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-2100.

Pranav Chandrasekhar
April 5,2004



THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100